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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,145	07/15/2003	Matthew A. Kliesner	72207	8483

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EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 10/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,145	KLIESNER ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,8,11,12,15 and 18* is/are rejected.

7)☒ Claim(s) *2,3,6,7,9,10,13,14,16,17,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 2 is objected to because of the following informalities: in line 4, "said one" should be changed to -- said another --. Appropriate correction is required.

2. Claim 3 is objected to because of the following informalities: in line 4, "said one" should be changed to -- said another --. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 4, 8, 11, 15 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang U.S. Patent 5,796,796 in view of admitted prior art.

Regarding claim 1, Wang invention is directed to method and apparatus for cancellation of pointer adjustment jitter by utilizing a phase hopping technique.

FIG. 2 shows a pointer adjustment jitter cancellation system 100 including an elastic buffer 110 for storing the incoming data stream according to a write clock signal; see column 6 lines 15-55.

Wang does not teach the elastic buffer 110 storing the incoming data stream according a data valid signal as claimed in the application claim.

In paragraph [0002] of the original disclosure, FIG. 1 admitted prior art of the original disclosure teaches a serial data stream 11 is clocked into a FIFO buffer 10 according to an incoming clock signal 12. As taught in admitted prior art, because the data is not necessary continuous, a valid data signal 13 indicating when the data is valid is provided to the buffer. For the aforementioned, since the data is not necessary continuous, one of ordinary skill in the art at the time the invention was made would have been motivated to modify teachings to implement a valid data signal, as taught in FIG. 1 admitted prior art, indicating when the data is valid to the elastic buffer 110.

The pointer adjustment jitter cancellation system 100 further includes a phase hopping control 150 shown in FIG. 3 for applying the write clock signal. The hopping control circuit 150 further includes a plurality of delay circuits 180-i, i=1, 2, 3, . . . , n, for receiving the write clock signal for generating a plurality of phase hopping delay signals wherein each of the delay circuits is provided for generating a phase hopping delay signals of approximately equal phase delay. The apparatus further includes a multiplexer 170 for receiving the phase hopping delay signals and the address from the up-down counter 160 to generate the read clock signal for controlling a data bit output from the elastic buffer 110. In view of the aforementioned teachings, output of MUX 170 corresponds to the claimed output port. See further in column 6 lines 15-55, also FIG. 2and 3.

Regarding claim 4, as discussed in paragraphs [0002] and [0003] of the original disclosure, see also FIG. 1, admitted prior art teaches that the output end 14 of the buffer requires the generation of a read clock 16 that matches the effective data rate, but without gaps such as may be associated with times of the input clock for which there is no valid data. In light of the teachings, the relationship between the valid data signal and the output clock signal is represented by the amount of data contained in the FIFO storage buffer and the data storage capacity of the FIFO storage buffer.

Regarding claim 8, claim is rejected on the same ground as for claim 1 because similar scope.

Regarding claim 11, claim is rejected on the same ground as for claim 4 because similar scope.

Regarding claim 15, claim is rejected on the same ground as for claim 1 because similar scope.

Regarding claim 18, claim is rejected on the same ground as for claim 4 because similar scope.

4. Claims 5 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang U.S. Patent 5,796,796 and admitted prior art as applied to claim 4 above, and further in view of Maas et al. U.S. Patent 6,092,128.

Regarding claim 5, Wang and FIG. 1 admitted prior art do not explicitly teach the relationship between said valid data signal and said output clock signal is represented an underflow or overflow condition of said FIFO storage buffer.

Maas et al. discusses conventional first-in first-out (FIFO) buffers may employ status flags to indicate when particular boundary conditions (such as full, empty, almost full, almost empty, overflow, underflow, etc.) are present; see column 1, lines 10-25. Because overflow and underflow conditions are known in the operation of conventional FIFO buffer and because, as taught in admitted prior art, the generation of a read clock 16 that matches the effective data rate, but without gaps such as may be associated with times of the input clock for which there is no valid data, one of ordinary skill in the art would have been motivated to implement the overflow and underflow status flags as discussed in Mass et al. invention.

Regarding claim 12, claim is rejected on the same ground as for claim 5 because similar scope.

Allowable Subject Matter

5. Claims 2-3, 6-7, 9-10, 13-14, 16-17 and 19-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Gersbach et al. U.S. Patent 5,245,637 discloses "Phase And Frequency Adjustable Digital Phase Lock Logic System".

Song U.S. Patent 6,917,660 B2 discloses "Adaptive De-skew Clock Generation".

Paul et al. U.S. Patent 6,810,098 B1 discloses "FIFO Read Interface Protocol".

Jeong U.S. Patent 7,100,066 B2 discloses "Clock Distribution Device And Method In Compact PCI Based Multi-Processing System".

Ferraiolo et al. U.S. Patent 5,220,581 discloses "Digital Data Link Performance Monitor".

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KCT

Khanh Tran
Primary Examiner